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MTCMOS DESIGN FOR EFFECTIVE VOLTAGE DROP CONTROL

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Abstract— Power reduction is one of the most significant challenges in designing today's advanced VLSI circuits. Power gating is a technique used in IC design to reduce power consumption by shutting off the current to parts of the circuits which are not in use. In MTCMOS, the large inrush current and ramp up time are arised. We are proposing a new analytical model considering package RLC parasitic for reducing the inrush current and ramp up time. It is possible by analyzing the impact of decoupling capacitances on ramp up time and inrush current. Unlike the previous power sequence method, we are proposing a different inrush current modeling. We can consider our framework as a conservative method to limit the inrush current. So the power up sequence generated by our proposed method can satisfy the inrush current constraint.

Keywords— Inrush Current, Low Power Design, Multi-Threshold Cmos(Mtcmos), Power Gating, Power-Up Sequence, Ramp-Up Time.

I. INTRODUCTION

Reducing power dissipation is one of the most principle subjects in VLSI design today. Scaling causes sub threshold leakage currents to become a large component of total power dissipation. In CMOS technology, leakage increases exponentially and becomes a significant drain on total power consumption. The leakage power is expected to reach more than 50% of total power in the 65nm technology.

Power reduction is one of the most significant challenges in designing today's advanced VLSI circuits. Low power designs are desirable for various reasons including competent energy and temperature characteristics, higher battery time for portable devices, and lower packaging and maintenance costs.

Power consumption and power dissipation are really two different things. Power consumption is the intended use of power; work is performed. Power dissipation is a function of efficiency. Both, however, are highly dependent on operating temperature, the semiconductor process that is used to make the device, operating frequency, level of activity, and operating voltage. Both can be reduced through intelligent design.

Considering that battery life is a huge factor in the mobile phone market (or any other portable device, for that matter), it is common sense that devices that use less power will extend battery life until the next charge. Intelligent design, coupled with chips that perform actions while consuming mere micro-amps (μA), can create a stellar device with a full complement of impressive and even life-changing features for the consumer. Just ten years ago the amount of power that makes up an entire power budget today would have been a negligible loss back then and of no concern. These days, design for power efficiency is much more aggressive. The multi-threshold CMOS (MTCMOS) technique employs high-transistors to implement always-on circuits, such as power switches, retention flip-flops, and always-on buffers, to minimize their leakage power consumption. The power up/down of a gated domain is controlled by turning the header (or footer) power switches on or off. These switches are parallel-connected between the mesh of the chip's true VDD (or ground) and the mesh of the gated domain's virtual VDD(or virtual ground). This power-switch fabric, also called a distributed sleep transistor network (DSTN [1]).

The number and size of the transistors used in the power switch fabric determine the voltage drop between the true VDD and the virtual VDD [4]–[5]. This voltage drop degrades circuit performance, and must be kept below a user-specified value. Using a larger number of power switches can achieve a smaller voltage drop at the expense of more area overhead. After the power switches are allocated, the sequence that turns on the power switches for a domain (called the power-up sequence) determines the voltage ramp-up time and the inrush current of the domain. The ramp-up time is the time during which the virtual VDD rises from ground level to the required operating level for active mode. The inrush current is the maximum transient current flowing through the power switches during the sleep-to-active mode transition.

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There is generally a trade off between the ramp-up time and the inrush current [6]–[9]. A short ramp-up time may incur a large inrush current. It is necessary to constrain the inrush current of a domain, as an excessive inrush current may lead to excessive IR drop in other active domains resulting in chip malfunction. For example, an on-chip low drop out (LDO) voltage regulator may fail to boot up due to its being incapable of handling an excessive current surge.

II. POWER RAMP-UP MODELING

During power-up, a power switch (PSW) behaves like a current source and remains in the saturation region for a while. The power-gated devices connected to the virtual rail VDDV behave like resistors until the virtual rail is charged to the normal operating voltage. We model a power switch as a voltage-dependent current source and a gate including wires as a lumped resistance and a lumped capacitance denote the times at which the associated power switch can be turned on.

We perform HSPICE simulation based on the accurate SPICE net list considering layout parasitic extraction and calibrate the values of load capacitance and load resistance to evaluate the effects on both voltage ramp-up time and inrush current. For each load capacitance ranging from10 to 1000 fF, the load resistance of each sub-circuit (out of 40 K sub-circuits) is varied from 10 to 10 K . For a simple MTCMOS design constructed using a TSMC 65 nm low power library [10], wherein 400 HDRSID0HVT header switches are connected in parallel and 40 K sub circuits are attached to the virtual VDD. The R_{on} , I_{dsat} and propagation delay of an HDRSID0HVT switch are 678Ω, 0.479 mA and 120 ps, respectively. The power grid resistance is set to 0.1 to compliant with the IR and EM requirement. Each sub circuit in the gated domain consists of an INVD24 inverter with 22.78 fF pin capacitance.

For a DSTN structure, all its power switches are parallel-connected to the power mesh and share the current supply of the power-gated domain. So after parallel connecting the resistance of all 40 K sub-circuits, their equivalent resistance may not vary too much even though the resistance of each sub-circuit varies a lot.

III. POWER SWITCH BANKING AND INRUSH CURRENT BUDGETING

An ideal power-up sequence control in accordance with the proposed algorithm when the fixed time interval is set to 10 ns. This experiment sets the inrush current constraint to 100 mA with the power supply voltage set to 1.2 V. After optimization, we insert delay elements to comply with a set of time slots. By specifying an upper bound on the inrush current without restricting the size of the power switch bank, the proposed frame work maximizes the number of power switches in a bank that can be turned on in a specified time interval.

The accumulated current gradually increases to a maximum value (137.5 mA at 46 ns) and subsequently decreases until the voltage reaches the normal operation voltage. The dashed line and the solid line were produced using the proposed framework with time intervals of 10 and 1 ns, respectively. The accumulated current is continually kept below a specified limit (100 mA). The voltage increases faster than that achieved using the existing Hamiltonian path method.

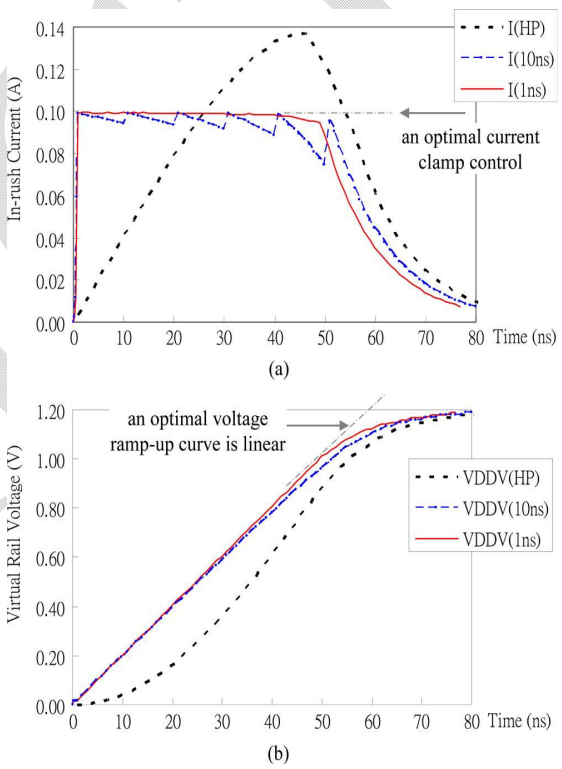

Fig. 1. ***Inrush current and voltage ramp-up profile using different power-up sequences.***

(a) Inrush current.

(b) Voltage ramp-up.

IV. DYNAMIC IR DROP MITIGATION

We employ a model based on to mitigate the dynamic IR drop on the active domains. First, power switches are weighted and ranked according to a function of their physical locations and that of DC sources. Then, they are clustered and routed according to the ranking guidance to prevent any excessive dynamic IR drop on the active domains.

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To identify the most fragile domain and its corresponding power mode that will suffer from the worst-case dynamic IR drop, we should take into account the locations of power domains and DC sources, the domains to be turned on simultaneously, the power mesh size as well as the capacitance of the gated circuit. Since it is computationally unaffordable to simulate every IR-drop map during the transition between every possible two adjacent power modes, we usually rely on designers' knowledge to designate numbers of power domains and power modes to analyze their worst-case IR drop.

In order to validate the correctness and the efficiency of the proposed switch ranking algorithm, we build an 80X80 true-VDD grid, where each unit grid has resistance of 0.1 The gated power-up domain and the active domain are connected to the bottom-right quarter and the top-left quarter of the true-VDD mesh, respectively. The gated power-up domain uses 40X40 TSMC 65 nm header switches (HDRSID2HVT). Estimated from a 65 nm, 1.2 V, 133 MHz 250 K-gate design, the gated domain is represented by a 1 nF capacitance and a 0.5 A current source connected to the virtual VDD. The R_{on} and I_{dsat} are 39.42Ω and 8.92 mA, respectively. We rank switches based on their $W(PS_i)$ values. Next, we perform SPICE simulation for the case that each switch is turned on independently with all other switches turned off and the initial virtual rail voltage is set to 0 V.

The switch with a larger rank (decreasing weight) produces a larger voltage drop on the active domain. Thus our ranking scheme can accurately predict a switch's effect on V (SP_i).

V. CONFIGURABLE DOMINO - DELAY CIRCUIT

Fig. 2 depicts a power-up sequence control system with a configurable domino-delay based on the proposed algorithm. The controller receives a sleep enable signal (denoted by SleepEn) and distributes the sleep enable outputs (denoted by SleepEnD [0-N]) in a domino fashion using a configurable time interval. The power switches are divided into several banks, which receive the controller's sleep enable signals according to the schedule. We place the controller in the power-gated domain. It cannot be interrupted by the system once it starts sending out power-on signals.

Our framework implements the domino-delay circuit after logic synthesis. We design a parameterized RTL code together with a Perl-script based circuit compiler to make the number of outputs and the time interval configurable. Although the implementation cannot be changed after synthesis, we keep the flexibility of dividing a 200 MHz (5 ns period) reference clock. The area overhead of the generated domino-delay controller is proportional to the number of output enable signals. In general, only about 400 gates are needed for a power-gated domain with 300 memory instances.

Each sleep enable output is supplied by a buffer tree, which may induce extra delay to the SleepEn signal. As a result, the switches are turned on a little later than our estimation model expects. It means that the actual inrush current is in fact smaller than that estimated by our inrush current model. In other words, our proposed inrush current model is a conservation one. As long as it can be satisfied, the actual in-rush current would be smaller than it reports. In our practical cases, the signal buffer tree is controlled within 5 levels, which may add around 0.5 ns delay (100 pS/level).

VI. POWER SWITCH ROUTING

Our framework generates a distributed routing topology for each power switch bank, wherein each power switch is sequentially connected to the next one. It observes both the maximum fan-out and maximum distance constraints between two adjacent power switches to prevent from happening design rule violations that would require extra always-on buffers to resolve. The maximum fan-out and maximum distance constraints ensure that neither the output loading of the current switch nor the input slew of the next routed switch exceed the upper bound set in the timing library.

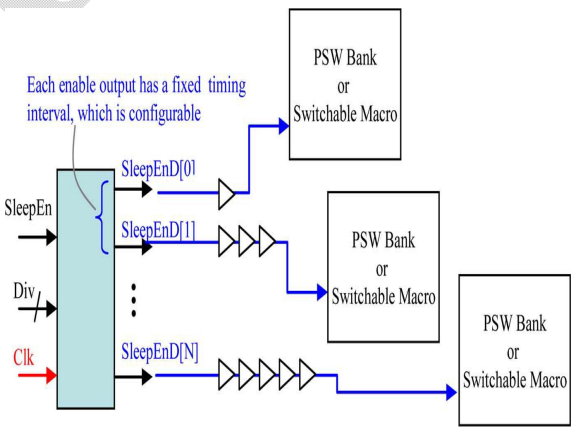

Fig. 2 : Configurable domino-delay control

Power switches are partitioned into several vertical banks within the specified horizontal search range *mFact*. The power switches in the same vertical banks are then further divided into disjoint sub banks to satisfy the maximum distance constraint MD. Within a vertical bank, the highest ranked switch is routed first.

The entry point or floating input of each vertical bank is connected to the nearest power switch of the adjacent bank.

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The floating input pin of a switch bank is subsequently patched by the nearest power switch in the adjacent bank at the corresponding vertical coordinate. Finally, an extra always-on buffer is inserted when a feasible driver cannot be found within the maximum distance constraint or the routing pattern violates the design rules.

VII. EXPERIMENTAL RESULTS

Three different methods were used to implement the power switch fabric. The first method (denoted as Parallel) employed a commercial automatic placement and route (APR) tool [11] to implement the power switch fabric in multiple short chains fashion with a delay inserted between two adjacent chains. The second method is the single-chained method based on finding a Hamiltonian-path (denoted as HP) [12].

The third method is the proposed framework with current limit set to 150 mA (denoted as B150 mA). This method initially sets the capacitances of the power-gated domains by assuming that 50% of the total capacitance of unknown nodes can be seen from the virtual rail. Ramp-up and dynamic IR analysis for the true VDD, the power switches, and the virtual rail, were performed using a commercial power analysis tool.

Table II lists the peak inrush current and the ramp-up time for each of the three power-gated domains (denoted as PD1, PD2, and PD3).

Compared to the Parallel method, the proposed framework can reduce the peak inrush current by 8.6 times.

TABLE I

PEAK CURRENT AND THE RAMP-UP TIME OF THE POWER-UP DOMAINS ASSOCIATED WITH DIFFERENT POWER-UP SEQUENCES

	peak inrush current (A)			time to 99%VDD (ns)		
Methods\Domains	PD1	PD2	PD3	PD1	PD2	PD3
Parallel	1.543	0.876	1.258	68	72	68
HP	0.182	0.147	0.165	467	407	412
B150mA	0.144	0.142	0.143	384	244	312
Comparison						
B150mA/Parallel	0.09	0.16	0.11	5.65	3.41	4.59
B150mA/HP	0.79	0.97	0.87	0.82	0.60	0.76

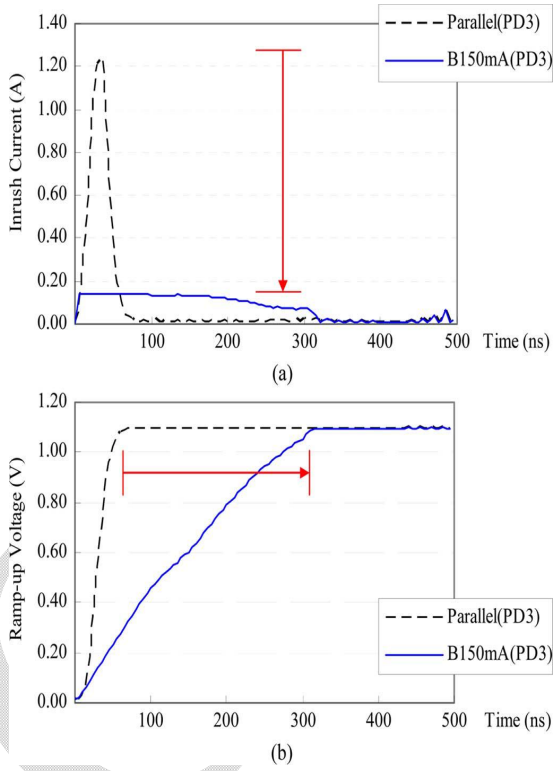

Fig. 3: ***Inrush current and voltage ramp-up profile of the PD3 power-up domain associated with the Parallel power-up sequences and the proposed framework, respectively.***

(a) Inrush current.
(b) Ramp-up voltage

While slowing down the ramp-up time by 4.5 times, as shown in Fig.3. Only 0.75% of area penalty is observed. Although the reference method may not meet the specified current limit, we showed this comparison because both methods turn on multiple power switches at the same time. The difference is that our proposed method can properly control the turn-on sequence of power switches while the reference method cannot.

VIII. CONCLUSION

In this paper, proposed a power-up sequence generation method to address the problem of minimizing ramp-up time under peak inrush current constraint for MTCMOS designs. The proposed framework includes a current budget algorithm based on an effective model, an analytical routing guidance and a configurable domino-delay controller. Experimental results demonstrate the effectiveness of the proposed framework in minimizing the ramp-up time while mitigating the dynamic IR effect on the active domains under a specified peak current limit.

This is not incorporated the effects of package model in this work. One necessary step in the future work is to explore an analytical model considering package *RLC* parasitic. For package selection and cost reduction, it is possible to extend our work to analyze the impact of decoupling capacitance on ramp-up time, inrush current and dynamic IR drop.

Considering the inductance imposed by the package would result in a different inrush current estimation. This can still consider this proposed framework as a conservative method to limit the inrush current since the package inductance will slow down the voltage ramp up and hence the actual inrush current will be smaller than our estimation. So the power-up sequence generated by our proposed method can still satisfy the inrush current constraint.

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